ABSTRACT

0053 A method and system for fabricating a capacitor utilized in a semiconductor device. A salicide gate is designated for use with the semiconductor device. A self-aligned contact (SAC) may also be configured for use with the semiconductor device. The salicide gate and the self-aligned contact are generally in a memory cell area of the semiconductor device to thereby permit the efficient shrinkage of memory cell size without an additional mask or weakening of associated circuit performance. Combining, the self-aligned contact and the salicide gate in the same memory cell area can effectively reduce gate resistance.